

Amendments to the Specification

Please replace the paragraph beginning on page 1, line 4 with the following amended paragraph:

The present invention relates to a digital-analog converting circuit (called D/A converting circuit, hereinafter), which may be incorporated in a semiconductor integrated circuit, having voltage-dividing ~~resistors~~ resistors.

Please replace the paragraph beginning on page 1, line 8 with the following amended paragraph:

Fig. 4 is an explanatory diagram schematically showing a construction of a conventional D/A converting circuit 40. The D/A converting circuit 40 is a circuit with a 3-bit resolution. Essentially, in the D/A converting circuit 40, $2^3=8$ ~~resistors~~ resistors R having equal resistant values are connected in series between a reference potential terminal Vref and a ground terminal GND. The reference potential terminal Vref supplies a reference potential. The ground potential supplies a ground potential. When a digital signal (code) is input to a decoder circuit (not shown), one of switches SW0 to SW7 is selected and is turned on under the control of the decoder circuit. One of levels of nodes N0 to N7 corresponding to the ON switch is output from an output terminal OUT through an amplifier AMP. Thus, the reference potential and the ground potential are equally divided into eight so as to convert the digital signal to a desired analog signal. A PMOS transistor PMOS is connected between the reference potential

terminal and the ~~resisters~~ resistors R. The PMOS transistor PMOS is a switch for inhibiting an operation of the circuit and for shutting off current consumption in response to an enable signal ENB.

Please replace the paragraph beginning on page 3, line 13 with the following amended paragraph:

According to an aspect of the invention, there is provided a digital-to-analog converting circuit that includes first and second potential terminals, an output node, first and second ~~resisters~~ resistors, first and second switches and a control circuit. The first ~~resisters~~ resistors are connected in series between a first node and the output node through first connecting points. Each of the first switches is connected between the first potential terminal and one of the first connecting points and the first node. The second ~~resisters~~ resistors are connected in series between a second node and the output node through second connecting points. Each of the second switches is connected between the second potential terminal and one of the second connecting points and the second node. The control circuit controls the first and second switches.

Please replace the paragraph beginning on page 5, line 1 with the following amended paragraph:

This embodiment has switches between a reference potential and voltage-dividing ~~resisters~~ resistors and between a ground potential and voltage-dividing

~~resisters~~ resistors. Thus, a constant potential can be applied to switches. No analog switch is used as the switch.

Please replace the paragraph beginning on page 5, line 10 with the following amended paragraph:

As shown in Fig. 1, the D/A converting circuit 10 includes a reference potential terminal Vref, a ground potential terminal GND, an amplifier AMP, an output terminal OUT, $(2^n-1)=7$ reference potential side ~~resisters~~ resistors R1, $(2^n-1)=7$ PMOS transistors P1 to P7, $(2^n-1)=7$ ground potential side resistors R2, and $2^n=8$ NMOS transistors N0 to N7. The reference potential terminal Vref supplies a reference potential. The ground potential terminal GND supplies a ground potential. The amplifier AMP amplifies analog signals. The output terminal OUT outputs analog signals. The reference potential side resistors R1 are connected in series between the reference potential terminal Vref and the output terminal OUT. The PMOS transistors P1 to P7 correspond to the reference potential side resistors R1. The ground potential side resistors R2 are connected in series between the ground potential terminal GND and the output terminal OUT. The NMOS transistors N0 to N7 correspond to the ground potential side resistors R2.

Please replace the paragraph beginning on page 6, line 2 with the following amended paragraph:

Sources of the reference potential side resistors R1 are connected to the reference potential terminal Vref . Drains of the reference potential side resistors R1 are connected to the output terminal OUT through the amplifier AMP. The gates of the reference potential side resistances R1 are connected to a decoder circuit 20, which will be described later. The reference potential side ~~resistors~~ resistors R1 have equal resistance values.

Please replace the paragraph beginning on page 6, line 23 with the following amended paragraph:

Sources of the ground potential side ~~resistors~~ resistors R2 are connected to the ground potential terminal GND. Drains of the ground potential side ~~resistors~~ resistors R2 are connected to the output terminal OUT through the amplifier AMP. The gates of the ground potential side ~~resistors~~ resistors R2 are connected to the decoder circuit 20, which will be described later. The ground potential side ~~resistors~~ resistors R2 have equal resistance values. The resistance values are equal to those of the reference potential side ~~resistors~~ resistors R1.

Please replace the paragraph beginning on page 7, line 7 with the following amended paragraph:

The NMOS transistors N0 to N7 function as switches for switching paths between the ground potential terminal GND and the ground potential side ~~resisters~~ resistors R2 and for changing the number of the ground potential side resistors R2 from zero to seven between the ground potential terminal GND and the output terminal OUT. In other words, one of the NMOS transistors N0 to N7 is turned on so that one of the paths can be selected between the ground potential terminal GND and the output terminal OUT. Thus, the number of the ground potential side resistors R2 between the ground potential terminal GND and the output terminal OUT is changed from one to seven.

Please replace the paragraph beginning on page 12, line 7 with the following amended paragraph:

As described above, according to this embodiment, the PMOS transistors P1 to P7 (reference potential side switches) are used for switching paths between the reference potential terminal Vref and the reference potential side ~~resisters~~ resistors R1. Therefore, all of the potentials to be applied to the PMOS transistors P1 to P7 are the reference potential and are common. Thus, the composite resistances of ON resistances are all constant in the PMOS transistors. The same is true in the NMOS transistors N0 to N7 (ground potential side switches). As a result, the precision of the

D/A conversion can be improved.

Please replace the paragraph beginning on page 12, line 23 with the following amended paragraph:

The size of each of the voltage-dividing resistors does not affect on the entire size of the D/A converting circuit 10 significantly. Therefore, increases in the numbers of the reference potential side ~~resisters~~ resistors R1 and the ground potential side ~~resisters~~ resistors R2 do not affect on the size of the D/A converting circuit 10 significantly.

Please replace the paragraph beginning on page 13, line 11 with the following amended paragraph:

All of the ~~resisters~~ resistors in the circuit have an equal size. Therefore, this embodiment is suitable for a semiconductor integrated circuit, which may be different in accordance with the production.

Please replace the abstract with the following amended abstract:

A digital-to-analog converting circuit includes first and second potential terminals, an output node, first and second ~~resisters~~ resistors, first and second switches and a control circuit. The first ~~resisters~~ resistors are connected in series between a first node and the output node through first connecting points. Each of the first switches is connected between the first potential terminal and one of the first connecting points and the first node. The second ~~resisters~~ resistors are connected in series between a second node and the output node through second connecting points. Each of the second switches is connected between the second potential terminal and one of the second connecting points and the second node. The control circuit controls the first and second switches.